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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/044,401 | 01/11/2002 | Eric R. DeLano | 10016664-1 | 8893 |

22879 7590 01/18/2005

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| EXAMINER | |
|---|---|
| LEE, CHRISTOPHER E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2112 | |

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/044,401 | DELANO, ERIC R. | |
| | Examin r | Art Unit | |
| | Christopher E. Lee | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sh et with the corr spondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8,10-14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the Amendment filed on 17th of September 2004. Claims 1, 12, 16 and 17 have been amended; claims 9 and 15 have been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 16th of June 2004. Currently, claims 1-8, 10-14, 16 and 17 are pending in this application.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 12, 16 and 17 recite the limitation "the width of the input port" and "the width of the output port" in lines 17-18 of the claim 12, in lines 22-23 of the claim 16, and in lines 13-14 of the claim 17, respectively. There is insufficient antecedent basis for these limitations in the claim, respectively. Therefore, the term "the width of the input port" and "the width of the output port" could be considered as --a width of the input port-- and --a width of the output port--, respectively, since those are not clearly defined in the claims.

### *Claim Rejections - 35 USC § 102*

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1, 3, 6-8 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yokoyama [JP 411296473 A; cited by the Applicant].

*Referring to claim 1,* Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1) for providing connections between a plurality of ports (e.g., DA I/O Board #1-#4 in Fig. 1) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) via a processing system (i.e., Crossbar Switch 5, Crossbar Switch I/O ports 6, Address Controller 8 and Data division 7 in Fig. 1) comprising: a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), said crossbar control data (i.e., discernment bits Sa and Sb, and Address) containing control information for formatting bit length of data (i.e., control information for configuring 128 bit or 256 bit port; See Fig. 24) from an input port (e.g., port for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as an input port, such that SW#2 being set '1' and SW#3 being set '1' make the port configure as an input port according to Figs. 3 and 11) to be transmitted to an output port (e.g., port for DA I/O Board #1-#4 in Fig. 1 configured as an output port, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) having less width than said input port (e.g., 256 bit board → 128 bit board in Fig. 24; See Paragraph [0149]).

*Referring to claim 3,* Yokoyama teaches at least one register (i.e., memory A 61-b1 and memory B 61c-1 in Fig. 9) on each input port and each said output port for storing data in memory (i.e., storing

configuration environment of the crossbar switch in the memory A, and partner's board name and port number in the memory B; See paragraphs [0076]-[0077]).

*Referring to claim 6,* Yokoyama teaches an input port and an output port (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as input ports, such that SW#2 being set '1' and SW#3 being set '1' making the port configure as an input port, and ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' making the port configure as an output port according to Figs. 3 and 11) of at least one of said plurality of ports (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1) are customized to have different widths (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

*Referring to claim 7,* Yokoyama teaches a plurality of said input ports (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as input ports, such that SW#2 being set '1' and SW#3 being set '1' make the port configure as an input port according to Figs. 3 and 11) are customized to have different width (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

*Referring to claim 8,* Yokoyama teaches a plurality of said output ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) are customized to have different width (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

*Referring to claim 11,* Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1) having a plurality of paths for providing connections (i.e., a plurality of communication paths among Processor Boards #1-#2, Memory Boards #1-#2 and DA I/O Board #1-#4 in Fig. 1) between a plurality of ports (e.g., DA I/O Board #1-#4 in Fig. 1) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) via a processing system (i.e., Crossbar Switch 5, Crossbar Switch I/O ports 6, Address Controller 8 and Data division 7 in Fig. 1) comprising: a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable

of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); a plurality of virtual communication channels (i.e., data paths by the interconnection of switches in Fig. 5) on each input port (i.e., on each data division 7-1 of Fig. 6); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from a virtual communication channel to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example).

*Referring to claim 12,* Yokoyama discloses a method for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), wherein said crossbar includes a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port

to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), said method comprising the steps of: receiving data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3); obtaining a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively); determining whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration); obtaining control information from said crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13); processing said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]); determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board); submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data); obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has

256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example); formatting said data from said input port to data configured for said obtained width of said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]); submitting said formatted data as said processed data; and, transmitting said processed data to a destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

*Referring to claim 13,* Yokoyama teaches reading control data received with said data on said input port (See Box S1 in Fig. 12 and col. 15, lines 41-45); determining whether said control data have valid port information (See Decision Box S2 in Fig. 12 and Decision Box S14 in Fig. 13 and paragraph [0098]; i.e., if a bit configuration information in said control data is not confirmed by OK from address line, then said control data has an invalid port information) and, aborting when said control data does not have valid port information (See Decision Box S16 and Box S17 in Fig. 13 and paragraph [0099]).

***Claim Rejections - 35 USC § 103***

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Applicant's Admitted Prior Art [hereinafter AAPA].

*Referring to claim 2,* Yokoyama discloses all the limitations of the claim 2 including said data received on said input port including control data for indicating destination information relating to data received on said input port (See paragraph [0080]), except that does not teach said data further comprising control data for indicating validity information relating to said data.

AAPA discloses a crossbar (Fig. 1), wherein said crossbar using control information from control data, which indicates validity information relating to data received on an input port (See page 5, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said validity information, as disclosed by AAPA, in said data received on said input port, as disclosed by Yokoyama, so as to verify the validity of port information relating to said data received on said input port, which is admitted by the applicant as well-known in the art (See AAPA, page 5, lines 13-19).

*Referring to claim 14,* Yokoyama discloses all the limitations of the claim 14 including obtaining said destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) from said control data (See paragraph [0080]), except that does not expressly teach said obtaining is performed when said control data has valid port information.

AAPA discloses a crossbar (Fig. 1), wherein obtaining a destination output port from said control data when said control data has valid port information (See page 5, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said validity information, as disclosed by AAPA, in said data received on said input port, as disclosed by Yokoyama, so as to verify the validity of port information relating to said data received on said input port, which is admitted by the applicant as well-known in the art (See AAPA, page 5, lines 13-19).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Tauchen et al. [US 6,411,230 B1; hereinafter Tauchen].

*Referring to claim 4,* Yokoyama discloses all the limitations of the claim 4 except that does not expressly teach at least one shift register on each input port for storing data in memory and shifting data with larger bit length to a smaller bit length data for transmission from an input port with more width to an output port with less width.

Tauchen discloses a circuit arrangement for parallel/serial conversion (See Abstract and Figure), wherein at least one shift register (i.e., first shift register 1 and second shift register 2 in Figure) on an input port for storing data in memory (See col. 3, lines 43-46) and shifting data with larger bit length to a smaller bit length data (See col.3, lines 62+; i.e., shifting $D_{Pin}$ with larger parallel bit length to a smaller serial bit length $D_{Sout}$ for Parallel/Serial conversion) for transmission from an input port with more width (i.e., a plurality of bits in parallel $D_{Pin}$ in Figure) to an output port with less width (i.e., a serialized bits $D_{Sout}$ in Figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said parallel/serial conversion, as disclosed by Tauchen, in said each input port of said crossbar, as disclosed by Yokoyama, for the advantage of performing the conversion of said input data (e.g., 256 bit width data; i.e., parallel data) into (e.g., 1 bit width data in serial; i.e., serial data) without needing any external software or microprocessor control (See Tauchen, col. 4, line 66 through col. 5, line 8) in addition to the fixed bit width crossbar switching (i.e., crossbar switching between 256 bit width and 128 bit width; See Yokoyama, Figs. 1 and 24).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Aimoto [US 6,570,876 B1].

*Referring to claim 5,* Yokoyama discloses all the limitations of the claim 5 except that does not expressly teach at least one multiplexor device on each said input port and each said output port for prioritizing transmissions of data.

Aimoto discloses a packet switch and switching method (See col. 1, lines 8-16 and Fig. 1), wherein at least one multiplexor device (i.e., relaying priority control unit 3 and received packet queuing unit 7 of input port interface 20 in Fig. 1, and transmission priority control unit 5 and transmission packet queuing unit 8 of output port interface 21 in Fig. 1) on each input port (i.e., input port interface 20 of Fig. 1) and

each output port (i.e., output port interface 21 of Fig. 1) for prioritizing transmissions of data (See col. 5, line 42 through col. 6, line 46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said multiplexor device, as disclosed by Aimoto, in said each input port of said crossbar, as disclosed by Yokoyama, for the advantage of providing crossbar switching (i.e., packet switching) that can perform both bandwidth control and priority control according to the communication protocol of variable length data (i.e., packet; See Aimoto, col. 2, lines 23-26).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Hsieh et al. [US 5,717,871 A; cited by the Applicant; hereinafter Hsieh].

*Referring to claim 10,* Yokoyama discloses all the limitations of the claim 10 except that does not expressly teach said crossbar control data contain control information for use by any one from the group of a shift register or a multiplexor device.

Hsieh discloses a programmable port for crossbar switch 10 in Fig. 1, wherein said programmable port receiving crossbar control data (See col. 9, lines 34-36) contain control information (See col. 9, lines 39-41) for use by any one from the group of a shift register (i.e., shift register 20 of Fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said programmable port, as disclosed by Hsieh, on said each port of said crossbar, as disclosed by Yokoyama, for the advantage of providing a port flexibility in the use of control inputs and reduces the number of crossbar switch control inputs required to implement various modes of port operation (See Hsieh, col. 2, lines 43-49).

11. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] in view of what was well known in the art, as exemplified by Lach [US 6,363,452 B1].

*Referring to claim 16,* Yokoyama discloses a system (i.e., crossbar switching system including in Fig. 1) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), wherein said crossbar includes a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1), and crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for indicating crossbar control information (i.e., Crossbar Switching control information) for transmitting data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), comprising: a storage medium (i.e., memory A 61b-1, and memory B 61c-1 in Fig. 9); a machine (i.e., means for switching in crossbar switch 5 of Fig. 1 for executing the flows in Figs. 12-15 and 17-23) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), said machine comprising a set of flow steps for: receiving data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in

Fig. 3); obtaining a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively); determining whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration); obtaining control information from said crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13); processing said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]); determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board); submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data); obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example); formatting said data from said input port to data configured for said obtained width of said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]); submitting said formatted data as said processed

data; and, transmitting said processed data to a destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Yokoyama does not expressly teach said machine comprising a set of instructions for said flow steps. The Examiner takes Official Notice that said flow steps could be achieved in all software implementation (i.e., instructions) with the same or equivalent results, using appropriate program codes (i.e., processor instructions), is well known to one of ordinary skill in the art, as evidenced by Lach, at col. 12, lines 3-9. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said flow steps , as disclosed by Yokoyama, in software since it would allow a better flexibility of an implementation than a hardware implementation.

*Referring to claim 17,* Yokoyama discloses a machine (i.e., means for switching in crossbar switch 5 of Fig. 1 for executing the flows in Figs. 12-15 and 17-23) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), said machine comprising a set of flow steps to: receive data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3); obtain a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively); determine whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration); obtain control information from a crossbar control data

when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13); process said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]); determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board); submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data); obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example); formatting said data from said input port to data configured for said obtained width of said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]); and submitting said formatted data as said processed data; and, transmitting said processed data to a destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Yokoyama does not expressly teach said machine comprising a set of instructions for said flow steps. The Examiner takes Official Notice that said flow steps could be achieved in all software implementation (i.e., instructions) with the same or equivalent results, using appropriate program codes (i.e., processor instructions), is well known to one of ordinary skill in the art, as evidenced by Lach, at col. 12, lines 3-9.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said flow steps , as disclosed by Yokoyama, in software since it would allow a better flexibility of an implementation than a hardware implementation.

***Response to Arguments***

12. Applicant's arguments filed on 17th of September 2004 have been fully considered but they are not persuasive.

*In response to the Applicant's argument with respect to* the Remarks on page 9, the Examiner respectfully recommends that the Applicant translates the Yokoyama reference in English for the benefit of the Applicant's position, which was cited by the Applicant. Basically, the Office does not provide an accurate translation service to the Applicant.

*In response to the Applicant's argument with respect to* "The objections to the claims, and particularly claims 12, 15-17, have been made to overcome these with the exception of the noted and amendments have been suggestion that the 'the width of the ... port' should be changed to 'a width of the ... port' because it is believed to be awkward and unnecessary. It is certainly known that a port has a width and antecedent basis should not be necessary in the context of these claims." on Response filed on 17th of September 2004 (hereinafter the Response), page 10, lines 7-12, the Examiner respectfully disagrees.

In contrary to the Applicant's assertion, the claimed subject matters "the width of the input port" and "the width of the output port" are indefinite for failing to particularly point out and distinctly claim the subject matters which the Applicant regards as the claimed invention. In other words, the width of the port is indefinitely pointing out the subject matters which the Applicant regards as the claimed invention. For example, the width of the port could be interpreted as (1) a width of the port bandwidth, (2) a width of the port bus (connector) width, (3) a width of the port in longitudinal, or (4) a width of the port in latitudinal, etc., by one of the ordinary skill in the art.

Thus, the Applicant's argument on this point is not persuasive.

*In response to the Applicant's argument with respect to* "With regard to amended claim 1, which now includes the subject matter of claim 9, ... The reliance on Fig. 24 is not instructive as it merely shows a table of control numbers, i.e., C1 through C9, which essentially seems to show that a 256 bit band can be secured for transmitting 128 bit or 256 bit data, with paragraph 0149 reading ... Nowhere else in the specification, to the extent that applicant can understand it, is there any discussion that data is formatted at all. ..." on the Response, page 10, line 19 through page 11, line 6, the Examiner believes that the Applicant misinterprets the claim rejection.

Actually, Yokoyama teaches discernment bits Sa and Sb, and Address in Fig. 2 (i.e., crossbar control data) contain control information for configuring (i.e., formatting) bit length of data, 128 bit or 256 bit, for port (i.e., control information for formatting bit length of data; Fig. 24 shows the example cases C1-C9 for the convenience of the explanation in the specification) from a port for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1, which is configured as an input port, such that SW#2 being set '1' and SW#3 being set '1' makes the port configure as an input port according to Figs. 3 and 11 to be transmitted to a port for DA I/O Board #1-#4 in Fig. 1, which is configured as an output port, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11 with less width than said input port (e.g., case of 256 bit board → 128 bit board in Fig. 24; See Yokoyama, Paragraph [0149]). Therefore, in contrary to the Applicant's statement, Yokoyama clearly suggests the claimed limitation, such that control information for formatting (i.e., configuring) bit length of data (i.e., control information for configuring bit length of data, 128 bit or 256 bit, for port).

Thus, the Applicant's argument on this point is not persuasive.

*In response to the Applicant's argument with respect to* "The subject matter of claim 15 has been added to claims 12, 16 and 17 and the examiner has commented with regard to claim 15 that Yokoyama meets the formatting step by Box S20 in Fig. 14, ... Paragraphs 0090-0091 in the computer-generated

translation read as follows: ... Clearly, these paragraphs cited by the examiner have nothing to do with the step of processing the data which comprises the steps of determining whether the width of the input port is more than the width of the output port, ..." on the Response, page 11, line 7 through page 12, line 6, the Examiner believes that the Applicant misinterprets the claim rejection.

Actually, Yokoyama teaches determining whether the communication partner is 128 bit configuration board or 256 bit configuration board, being checked by Decision Blocks S2 and S6 in Fig. 12 (i.e., whether a width of said input port is more than a width of said output port); determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data, being processed by Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 (See Yokoyama, col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., submitting said data as a processed data when said width of said input port is not more than said width of said output port); determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example, being processed by Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 (See Yokoyama, col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., obtaining said width of said output port when said width of said input port is greater than said width of said output port); formatting said data from said input port to data configured for said obtained width of said output port (See Yokoyama, paragraphs [0090]-[0091]; i.e., wherein in fact that it checks about the signal from the address control section in a board with reference to the path and phase hand information in the Memory B during the data transfer impliedly suggests said data from said input port being formatted to data configured for said obtained width of said output port, e.g., case of 256 bit board → 128 bit board in Fig. 24; See Box S20 in Fig. 14); and, submitting said formatted data as said processed data (See Yokoyama, Box S21 in Fig. 14 and col. 17, lines 10-14).

Thus, the Applicant's argument on this point is not persuasive.

*In response to the Applicant's argument with respect to* "Claim 11 is also believed to be allowable for the reason that Yokoyama totally fails to anticipate, teach or suggest a crossbar having a plurality of virtual communication channels on each input port. The examiner attempts to equate a plurality of virtual communication channels on each input port to data paths that are provided by the interconnection of switches in Fig. 5. Applicant believes that this is a totally misplaced reliance on the switch configuration shown in Fig. 5. It has nothing to do with virtual communication channels that are claimed." on Response page 1, lines 10-20, the Examiner respectfully disagrees.

In fact, the Applicant recites the claimed limitation "a plurality of virtual communication channels on each input port" in the claim 11, line 7. However, it is noted that the features upon which applicant relies (i.e., something to do with said virtual communication channels) are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, the Applicant's argument on this point is not persuasive.

***Conclusion***

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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